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October 1987
Revised January 1999

MM74C150 • MM82C19
16-Line to 1-Line Multiplexer 3-STATE • 16-Line to 1-Line Multiplexer

General Description

The MM74C150 and MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

A strobe override places the output of MM74C150 in the logical "1" state and the output of MM82C19 in the high-impedance state.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

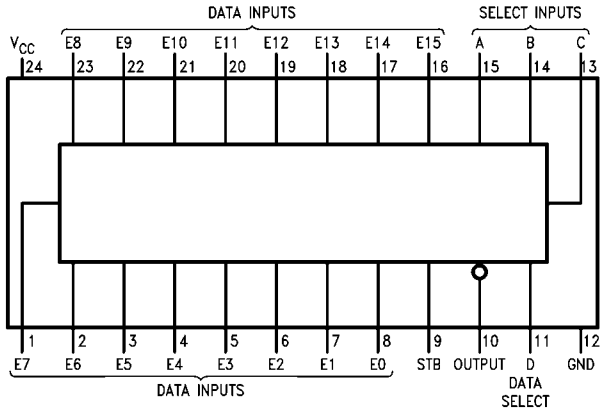
- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- TTL compatibility: Drive 1 TTL Load

Ordering Code:

Order Number	Package Number	Package Description
MM74C150N	N24A	24-Lead plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
MM82C19N	N24A	24-Lead plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Connection Diagram

Pin Assignments for DIP



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Truth Table

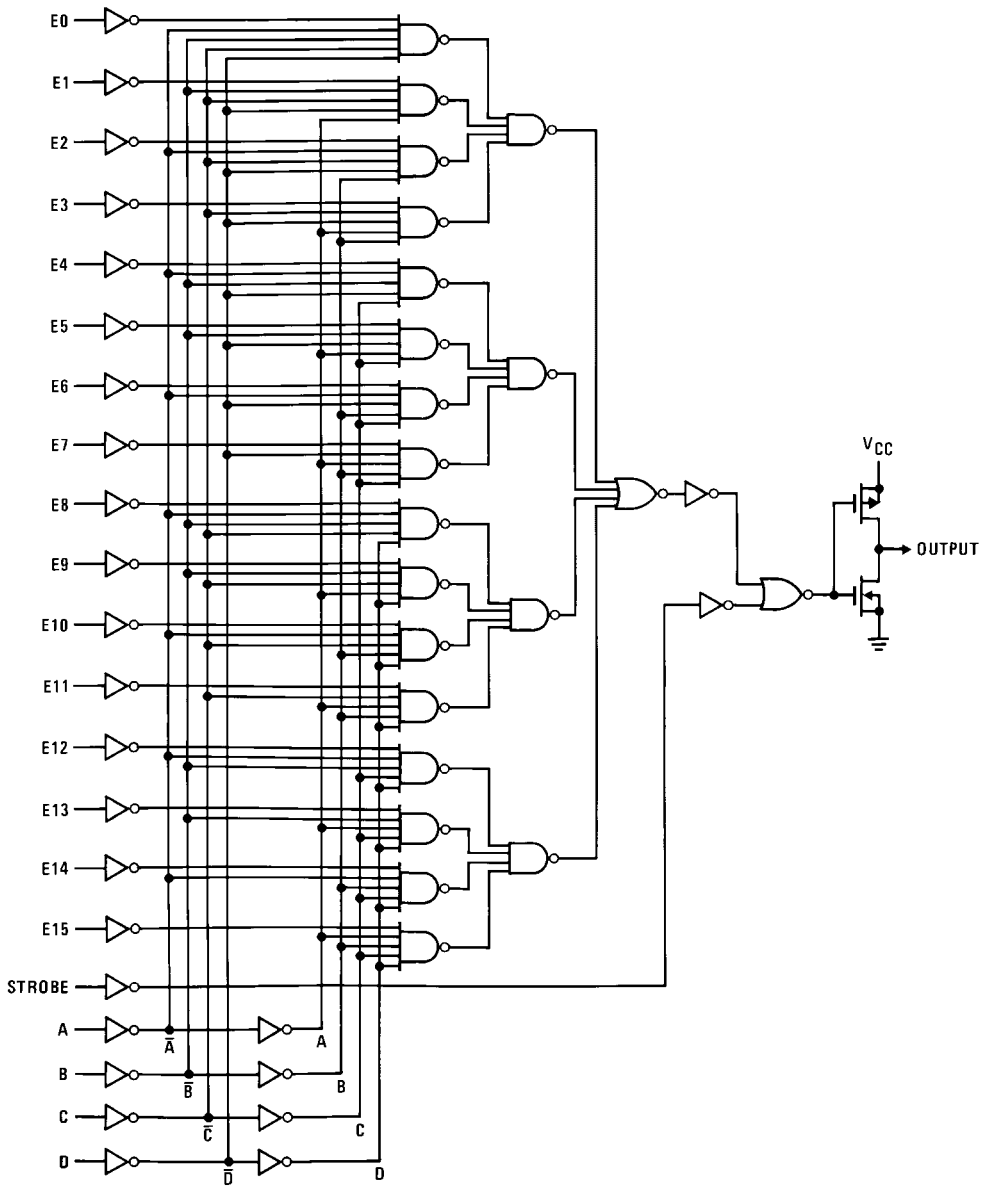
MM74C150

Inputs																				Output
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 (Note 1)
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

Note 1: For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

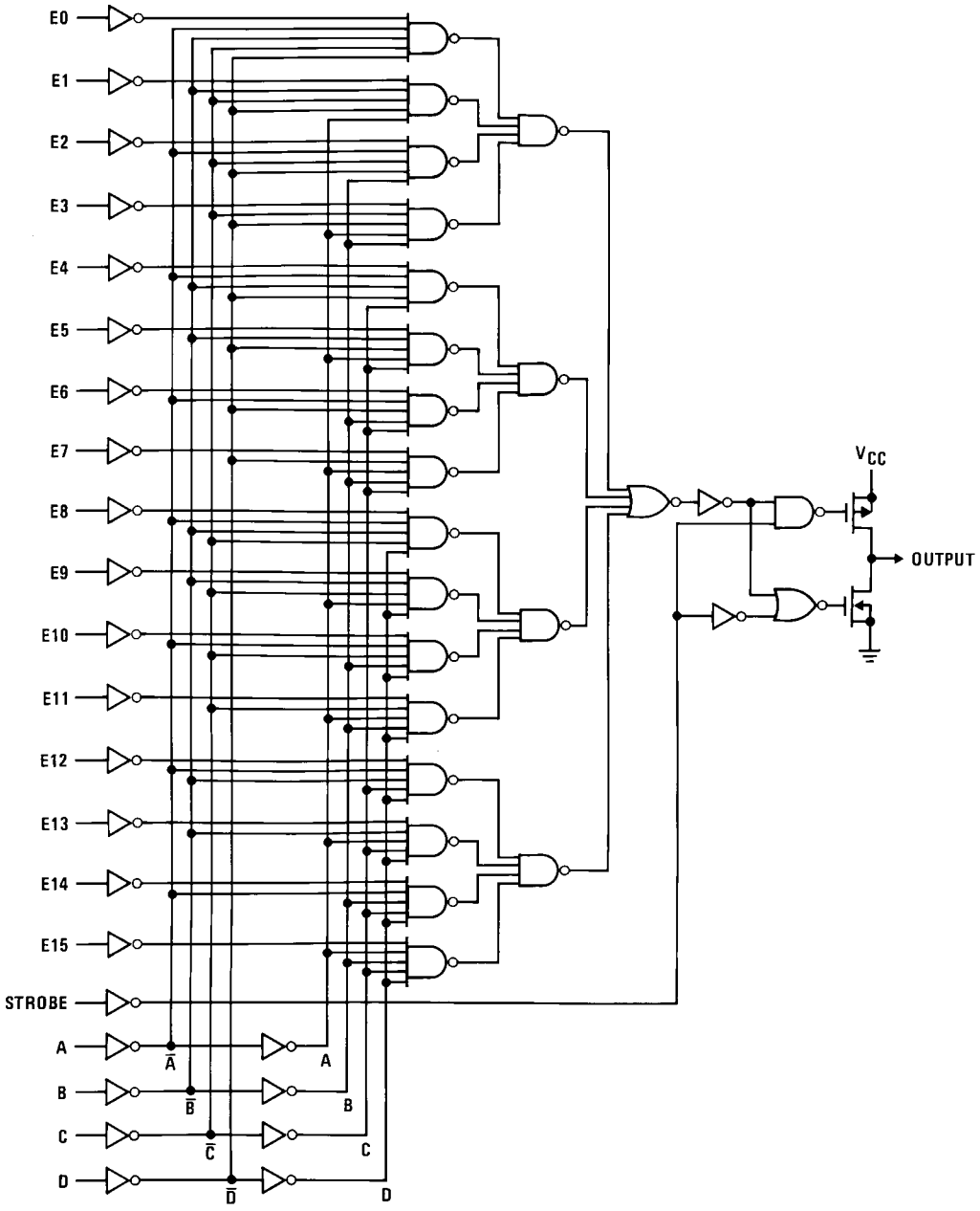
Logic Diagrams

MM74C150



Logic Diagrams (Continued)

MM82C19



Absolute Maximum Ratings(Note 2)

Voltage at Any Pin	−0.3V to V_{CC}+0.3V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature	
(soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristic table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 µA	4.5			V
		V_{CC} = 10V, I_O = −10 µA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10 µA			0.5	V
		V_{CC} = 10V, I_O = +10 µA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	V
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{OZ}	Output Current in High Impedance State					
	MM82C19	V_{CC} = 15V, V_O = 15V		0.005	1.0	µA
		V_{CC} = 15V, V_O = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	µA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	74C, 82C, V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	74C, 82C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	74C, 82C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	74C, 82C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−4.35	−8		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−20	−40		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	20	40		mA

AC Electrical Characteristics (Note 3)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a	$V_{CC} = 5.0V$		250	600	ns
	Logical "0" or Logical "1"	$V_{CC} = 10V$		110	300	ns
	from Data Inputs to Output	$V_{CC} = 5.0V$, $C_L = 150$ pF		290	650	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a	$V_{CC} = 5.0V$		290	650	ns
	Logical "0" or Logical "1"	$V_{CC} = 10V$		120	330	ns
	from Data Select Inputs to					
	Output					
t_{pd0}, t_{pd1}	Propagation Delay Time to a	$V_{CC} = 5.0V$		120	300	ns
	Logical "0" or Logical "1"	$V_{CC} = 10V$		55	150	ns
	from Strobe to Output					
	MM74C150					
t_{1H}, t_{0H}	Delay from Strobe to High	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF		80	200	ns
	Impedance State	$V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		60	150	ns
	MM82C19					
t_{H1}, t_{H0}	Delay from Strobe to Logical	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF		80	250	ns
	"1" Level or to Logical "0"	$V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		30	120	ns
	Level (from High Impedance State)					
	MM82C19					
C_{IN}	Input Capacitance	Any Input (Note 4)		5.0		pF
C_{OUT}	Output Capacitance	(Note 4)		11.0		pF
	MM82C19					
C_{PD}	Power Dissipation Capacitance	(Note 5)		100		pF

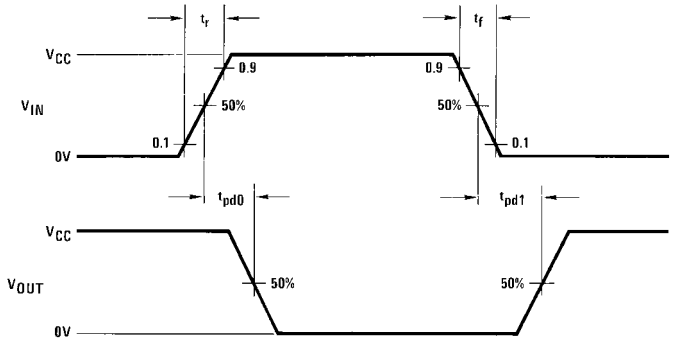
Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

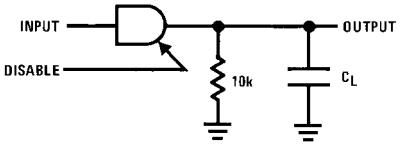
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics, application note AN-90.

Switching Time Waveforms

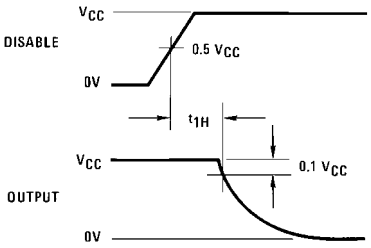
CMOS to CMOS



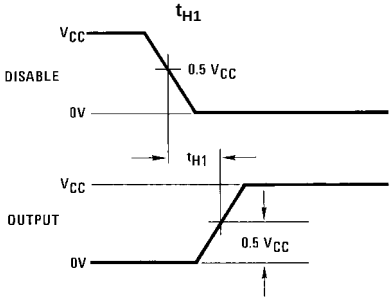
t_{1H} and t_{H1}



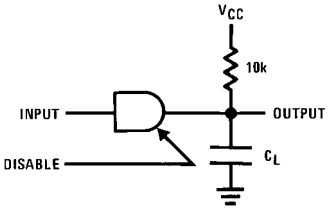
t_{1H}



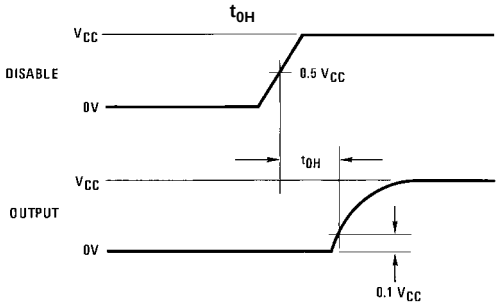
t_{H1}



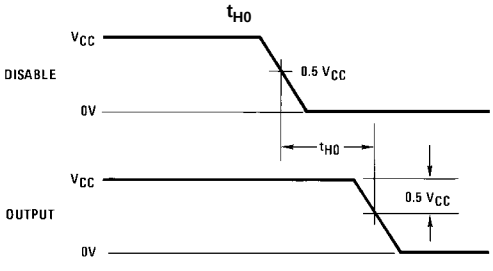
t_{0H} and t_{H0}



t_{0H}

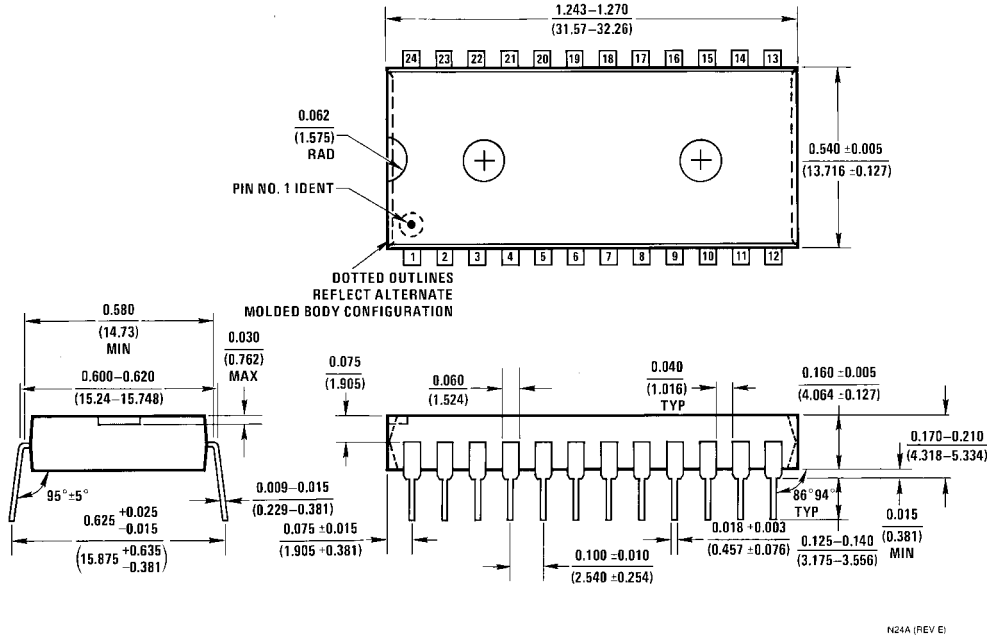


t_{H0}



Note: Delays measured with input t_r, $t_f \leq 20$ ns.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
Package Number N24A

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